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#### **REMARKS**

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

#### **Status of Claims**

Claims 1-44 are pending in the application. Claims 1-44 have been rejected. Claims 1, 12, 23 and 34 have been amended.

Applicants respectfully assert that the amendments to claims, the specification and the drawings add no new matter.

#### **Remarks to the Drawings**

Fig. 7 has been amended as requested by the Examiner to correct a reference numeral error. The entire drawing sheet containing each corrected drawing is enclosed for review by the Examiner.

#### **Remarks to the Specification**

The specification has been amended to make the specification conform with amended Fig. 7 of the drawing figures. Specifically, in the paragraph beginning in page 22 line 22, the words "decoders 104 and 106" has been replaced with the words "decoder 104" to make the specification conform with Amended Fig. 7. Additionally, in the paragraph beginning in page 23, line 18, the words "decoders 104/106" have been replaced with the words "decoders 104 and 106" to clarify which decoders are being referred to in the paragraph.

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The amendments to the specification are editorial in nature and do not introduce new matter. The Examiners approval of the amendments to the specification is respectfully requested.

### **Objections to the Drawings**

The drawings have been objected to for failing to comply with 37CFR 1.84(p)(4) because reference characters "104" and "106" have been used to designate the decoding system of Fig. 7. Applicant has amended Fig. 7 by deleting the redundant reference numeral "106". The Examiner's objection to the drawings is now cured. The Examiner's approval of Amended Fig. 7 is respectfully requested.

### **CLAIM REJECTIONS**

#### **35 U.S.C. § 102 Rejections**

In the Office Action, the Examiner rejected claims 1,12,23,24,26,27,34,35,37 and 38 under 35 U.S.C. § 102(b), as allegedly being anticipated by Sauer et al. (U.S. #5,973,311). Applicant respectfully traverses the Examiner's rejection in view of the remarks that follow. However, in order to expedite prosecution applicant has amended independent claims 12 and 24.

Applicant respectfully asserts that Sauer et al. do not teach nor even fairly suggest all the elements recited in in amended independent claims 1, 12, 23 and 34.

Moreover, Applicant asserts that the circuits taught by Sauer et al. do not perform the "summing charge from one or more of said unit cells" as recited in amended independent claims 1 and 23, nor do they perform the "by summing the charge generated by one or more unit cells of said plurality of unit cells" as recited in amended independent claims 12 and 34. The Examiner's attention is directed to Fig. 3 of Sauer et al. The circuit described by Sauer et al. uses source follower circuits including transistors TB1 and TB2 to isolate the pixel

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elements FD11 and FD12 from the output signal line 30. Transistors TS1, and TS2 of Fig. 3 of Sauer et al. are NMOS transistors acting as ON/OFF switches (low-impedance/high-impedance, respectively) controlled by ROW SELECT LINE 1 and ROW SELECT LINE 2, respectively.

The transistors TS1 and TS2 act as switches. In high-resolution mode either TS1 is ON and TS2 is OFF, or vice versa. In high-resolution mode the output signal is generated either from SIGNAL LINE 1, or from SIGNAL LINE 2, but not from both.

Since buffer transistor TB1 is configured as a source follower (as described multiple times in the specification of Sauer et al., for example, see column 5, lines 50-52, column 5, lines 64-67 and column 6, lines 6-8 of Sauer et al.), it isolates the input (SIGNAL LINE 1 connected to the gate of transistor TB1) from the output (the Source node of buffer transistor TB1). The buffer transistor TB1 presents a high input impedance to the FD11 output, thus preventing it being loaded by the OUTPUT SIGNAL LINE impedance (which might affect the FD11 signal due to its relatively low impedance).

The source follower's output signal is approximately equal to  $v_{SL1}$  (as the source signal follows the gate signal), however the output impedance of transistor TB1 is substantially lower than the output impedance of the pixel FD11. Therefore, the output signal on the OUTPUT SIGNAL LINE 30 is a voltage approximately equal to the voltage of SIGNAL LINE 1. The Examiner's attention is directed to the fact that the charge accumulation capacitor C11 of pixel FD11 stays charged (is not discharged) during the signal sensing process.

Similarly, if switching transistor TS1 is OFF and switching transistor TS2 is ON, the output signal on the OUTPUT SIGNAL LINE 2 is a voltage approximately equal to the voltage of SIGNAL LINE 2. The Examiner's attention is again directed to the fact that the charge accumulation capacitor C12 of pixel FD12 stays charged (is not discharged) during the signal sensing process.

However, in the low-resolution mode of the Sauer et al imager, both switching transistor TS1 and switching transistor TS2 are ON and the output signal is simultaneously generated from both SIGNAL LINE 1 and SIGNAL LINE 2.

Typically, a source follower (such as the buffer transistors TB1 and TB2 of Sauer et al.) works properly whenever its output impedance is low in comparison to the output load.

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However, in Figure 3 of Sauer et al., in the low resolution mode (when both TS1 and TS2 are ON), one source follower output impedance loads the other source follower. This results in outputting a voltage signal that is approximately half the sum of the SIGNAL LINE 1 voltage and the SIGNAL LINE 2 voltage. In other words, when the Sauer et al. circuit of Fig. 3 operates in the low resolution mode, the output voltage  $V_{out}$  on the output signal line 30 is :

$$V_{OUT} \cong \frac{Q11 + Q12}{2 \cdot C11}$$

wherein,

Q11 is the charge accumulated on capacitor C11,

Q12 is the charge accumulated on capacitor C12, and

$C11 \cong C12$  is the capacitance of the capacitors C11 and C12

Applicant therefore asserts that in the circuit disclosed by Sauer et al. when operated in the low-resolution mode, the output signal is proportional to the average of the accumulated charges of pixel elements FD11 and FD12 and not to the true sum of the accumulated charges.

Applicant asserts that the circuits disclosed by Sauer et al. perform a charge averaging step and therefore cannot and do not perform true charge summing as is performed by the direct injection unit cells of the circuits taught by the present invention. Therefore, the circuits disclosed by Sauer et al. do not teach or even fairly suggest the step of "summing charge from one or more of said unit cells" as claimed in amended claims 1 and 23 or the step of "summing the charge generated by one or more unit cells of said plurality of unit cells" as claimed in amended claims 12 and 34.

Moreover, applicant asserts that the charge averaging circuit as disclosed by Sauer et al. teaches away from Applicant's circuit which is configured to perform true charge summing of the direct injection unit cells of the present invention.

In view of the above remarks, Applicant respectfully asserts that amended independent claims 1, 12, 23, and 34 are allowable. Claims 24, 26, 27 depend from, directly or indirectly, amended claim 34 and therefore include all the limitations of this claim and are

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also allowable. Claims 35,37 and 38 depend from, directly or indirectly, amended claim 34 and therefore include all the limitations of this claim and are also allowable.

Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections under 35 U.S.C. § 102(b) to amended independent claims 1 and to amended independent 23 and to claims 24,26,27, dependent thereon.

Similarly, for the same reasons indicated hereinabove, Sauer et al. cannot anticipate claims 12 and 34 as amended. Applicant respectfully requests that the Examiner withdraw the rejections under 35 U.S.C. § 102(b) to amended independent claim 12 and to amended independent 34 and to claims 35,37 and 38 dependent thereon.

Applicants respectfully request reconsideration and withdrawal of the rejections of claims 1,12,23,24,26,27,34,35,37 and 38.

### **35 U.S.C. § 103 Rejections**

In the Office Action, the Examiner rejected claims 2,4,5,13,15 and 16 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Kokie et al. (US #4,212,034)

Applicants respectfully traverse the rejection of claims 2,4,5,13,15 and 16 as being unpatentable over Sauer et al. in view of Kokie et al. (US #4,212,034) because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention. The combination of Sauer et.al. and Kokie et al., does not teach or even fairly suggest all the limitations of independent claim 1 or of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 2,4,5 and 13,15,16 depending, respectively, thereon. Sauer et al. has been discussed above. That discussion is applicable here. Applicant respectfully asserts that since the Sauer et al. circuit teaches away from charge summing, the man skilled in the art would not have been motivated to combine Kokie et al. with Sauer et

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al., as there would be no motivation to combine the circuits taught by Kokie et al with the charge averaging circuit of Sauer et al which teaches away from charge summing. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 3 and 14 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Kokie et al. and further in view of Pain et al. (US #8,801,258).

Applicants respectfully traverse the rejection of claims 3 and 14 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Kokie et al. and further in view of Pain et al. (US #8,801,258), because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention. The combination of Sauer et al., Kokie et al., and Pain et al. does not teach or even fairly suggest all the limitations of independent claim 1 or of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 3 and 14 depending, respectively, thereon. Sauer et al. and Kokie et al. have been discussed above. That discussion is applicable here. Applicant respectfully asserts that since the Sauer et al. circuit teaches away from charge summing, the man skilled in the art would not have been motivated to combine Kokie et al. and Pain et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Kokie et al. and Pain et al. with the charge averaging circuit of Sauer et al. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 6, 7, 17, 18 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al., Kokie et al., Pain et al., and further in view of Nishida et al. (US#4,996,600).

Applicants respectfully traverse the rejection of claims 6, 7, 17, 18 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al., Kokie et al., Pain et al. and further in view of Nishida et al. (US#4,996,600), because a prima facie case of obviousness has not been established.

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In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

The combination of Sauer et.al., Kokie et al., Pain et al. and Nishida et al. does not teach or even fairly suggest all the limitations of independent claim 1 or of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 6,7 and 17,18 depending, respectively, thereon. Sauer et al., Kokie et al. and Pain et al. have been discussed above. That discussion is applicable here.

The combination of Sauer et.al., Kokie et al., and Pain et al. and Nishida et al. does not teach or even fairly suggest all the limitations of amended independent claim 1 or of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 3 and 14 depending, respectively, thereon. Sauer et.al., Kokie et al., and Pain et al. have been discussed above. That discussion is applicable here. Applicant respectfully asserts that since the Sauer et al. circuit teaches away from charge summing, the man skilled in the art would not have been motivated to combine Nishida et al, Kokie et al. and Pain et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Nishida et al., Kokie et al. and Pain et al. with the charge averaging circuit of Sauer et al. Accordingly, Applicants respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 8-11, 19-22 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Kokie et al. and further in view of Nishida et al.(US#4,996,600).

Applicants respectfully traverse the rejection of claims 8-11, 19-22 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Kokie et al. and further in view of Nishida et al.(US#4,996,600), because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

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The combination of Sauer et.al., and Kokie et al., and Nishida et al. does not teach or even fairly suggest all the limitations of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 8-11, 19-22 depending, respectively, thereon. Sauer et al., and Kokie et al. have been discussed above. That discussion is applicable here.

The combination of Sauer et.al., Kokie et al. and Nishida et al. does not teach or even fairly suggest all the limitations of amended independent claim 1 or of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 8-11 and 19-22 depending, respectively, thereon. Sauer et.al., Kokie et al., and Pain et al. have been discussed above. That discussion is applicable here. Applicant respectfully asserts that since the Sauer et al. circuit teaches away from charge summing, the man skilled in the art would not have been motivated to combine Nishida et al, Kokie et al. and Pain et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Nishida et al., Kokie et al. and Pain et al. with the charge averaging circuit of Sauer et al. Accordingly, Applicants respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 25, 36 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Pain et al.

Applicants respectfully traverse the rejection of claims 25, 36 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Pain et al., because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

The combination of Sauer et.al., and Pain et al., does not teach or even fairly suggest all the limitations of amended independent claim 23, and 34 nor does it teach or suggest all the limitations of dependent claims 26 and 36 depending, respectively, thereon. Sauer et al. has been discussed above. That discussion is applicable here.



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Applicant respectfully asserts that since the Sauer et al. circuit teaches away from charge summing, the man skilled in the art would not have been motivated to combine Pain et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Pain et al. with the charge averaging circuit of Sauer et al. Accordingly, Applicants respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 28, 29, 39, 40 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Pain et al., and further in view of Nishida et al.

Applicants respectfully traverse the rejection of claims 28, 29, 39, 40 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and pain et al., and further in view of Nishida et al. because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

The combination of Sauer et.al., Pain et al., and Nishida does not teach or even fairly suggest all the limitations of amended independent claim 23, and 34 nor does it teach or suggest all the limitations of dependent claims 28-29 and 39-40 depending, respectively, thereon. Sauer et al. and Pain et al. has been discussed above. That discussion is applicable here.

Applicant respectfully asserts that since the Sauer et al. circuit teaches away from charge summing, the man skilled in the art would not have been motivated to combine Pain et al. and Nishida et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Pain et al. and Nishida et al. with the charge averaging circuit of Sauer et al. Accordingly, Applicants respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

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In the Office Action, the Examiner rejected claims 30-33, 41-44 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Nishida et al.

Applicants respectfully traverse the rejection of claims 30-33, 41-44 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Nishida et al. because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

The combination of Sauer et al., and Nishida does not teach or even fairly suggest all the limitations of amended independent claim 23, and 34 nor does it teach or suggest all the limitations of dependent claims 30-33 and 41-44 depending, respectively, thereon. Sauer et al. has been discussed above. That discussion is applicable here.

Applicant respectfully asserts that since the Sauer et al. circuit teaches away from charge summing, the man skilled in the art would not have been motivated to combine Nishida et al. with Sauer et al., as there would be no motivation to combine the circuits taught Nishida et al. with the charge averaging circuit of Sauer et al. Accordingly, Applicants respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

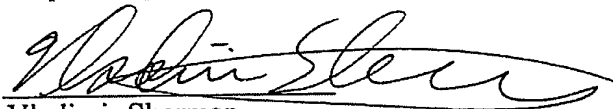
In view of the foregoing amendments and remarks, all pending claims, claims 1-44 are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

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Please charge any fees associated with this paper to deposit account No. 50-3400.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Vladimir Sherman', written over a horizontal line.

Vladimir Sherman  
Attorney for Applicant(s)  
Registration No. 43,116

Dated: April 19, 2005

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#### **AMENDMENTS TO THE DRAWINGS**

The attached sheet of drawings includes changes to Fig. 7. This sheet, which includes Fig. 7, replaces the original sheet including Fig. 7. In Figure 7, redundant reference numeral 106 is omitted.

Attachment: Replacement Sheet  
Annotated Sheet Showing Changes

8/10

104  
104/106

FIG. 7

